TITLE OF THE INVENTION

A CIRCUIT FOR CONTROLLING A SELF-REFRESH PERIOD IN A
SEMICONDUCTOR MEMORY DEVICE

BACKGROUND OF THE INVENTION

5   The present invention relates to a semiconductor memory
device, and more particularly to a circuit for controlling a self-
refresh period to determine the period of the self-refresh
operation in the semiconductor memory device.

       Generally, the refresh operation should be continuously
10   performed during the stand-by mode of the memory device that
requires the refresh operation to keep data stored in the memory
cell of a DRAM device (DRAM: Dynamic Random Access Memory). The
refresh operation used for such an object is called "self-
refresh". Recently, the power supply voltage of the memory device
15   lowers, so that a current consumption therein must be reduced.
Accordingly, the self-refresh operation should be performed with
the minimum current consumption. In order to reduce the current
consumption for the self-refresh operation, it is desirous to
perform the self-refresh operation with the longest period as long
20   as the data retention time of the memory cell in the memory device
is satisfied. According to this fact, the period control circuit
for the self-refresh operation that can program the period of the
refresh operation up to an optimum level is widely used. The
period of the self-refresh operation is determined by selecting

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a pulse train having the longest period to satisfy a data retention time among a number of pulse trains output from a timer as a master clock, after measuring the data retention time of the memory cell in the memory device. The preferred embodiment of such

5   an art is disclosed in detail in Korea patent application No. 93-10315 filed by the same applicant.

In general, the data retention capability of the memory cell is closely related with the level of a power supply voltage and an ambient temperature. That is, if the power supply voltage

10 lowers or if the ambient temperature rises, the data retention capability of the memory cell is deteriorated. Therefore, the refresh operation should be more frequently performed when the power supply voltage is low. Further, the refresh operation should be more frequently performed when the ambient temperature is high.

15 The period control circuit for controlling the self-refresh operation of which period is variable according to the variation of the ambient temperature, is disclosed in the pages 43 and 44 of a publication entitled "SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS" published in 1993. According to such an art, the

20 variation of the ambient temperature is detected by using a polysilicon resistor and a well resistor having different resistance-temperature coefficients from each other, and a differential amplifier that is capable of sensing the voltage difference generated between the polysilicon resistor and the well

25 resistor. Further, according to the above mentioned fact, the period of the self-refresh operation is controlled by selecting one of the timers which output predetermined different period pulse trains suitable for the level of the ambient temperature.

However, even if the conventional self-refresh period control

30 circuit controls the period of the refresh operation responding to the ambient temperature of the memory device, the circuit can't control the period of refresh operation responding to the

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variation of the power supply voltage provided to the memory device.

In addition, the conventional self-refresh period control circuit has the problem that it is difficult to obtain the master clock having a period which approximates to the data retention time of the memory cell. That is, after the conventional timer circuit generates a number of pulse trains having different periods from each other(for example, $2\mu s$, $4\mu s$, . . . $128\mu s$, $256\mu s$) by frequency-dividing the pulse train output from an oscillator, the timer circuit selects one of the pulse trains as the self-refresh master clock. Since each pulse train has the relationship of the frequency-dividing, the timer circuit can't select a specific pulse train having an appropriate period between any one period and the next period(for example, between the $128\mu s$ and the $256\mu s$) as the master clock. Further, to form the pulse train having the appropriate period, even if the specific period can be selected as the master clock, another complicated timer circuit is necessitated in the conventional art.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a period control circuit for a self-refresh operation in a semiconductor memory device which reduces a current consumption by optimizing the period of the self-refresh operation.

It is another object of the present invention to provide a period control circuit for a self-refresh operation in a semiconductor memory device, wherein the period of a self-refresh operation is automatically varied according to variations of an ambient temperature of the memory device and a power supply voltage provided thereto.

It is still another object of the present invention to provide a period control circuit for a self-refresh operation in a semiconductor memory device which can optimize the period of a refresh operation to approximate to a data retention time of the 5 memory cell.

To achieve these objects, the period control circuit for the self-refresh operation disclosed in the present invention includes pulse generating means for outputting a predetermined periodic pulse train responding to an external control signal; frequency-dividing means for outputting a number of pulse trains which have different periods from each other by frequency-dividing said pulse train output from said pulse generating means; at least one temperature detecting means for outputting a temperature detection signal by detecting that the ambient temperature of said memory 15 device reaches at a predetermined level; at least one voltage detecting means for outputting a voltage detection signal by detecting that the power supply voltage applied to said memory device reaches at a predetermined level; combination pulse train generating means for outputting a number of combination pulse 20 trains by combining the said pulse trains output from said frequency-dividing means; and pulse selecting means for outputting a self-refresh master clock by selecting one of said combination pulse trains responding to said voltage detection signal and said temperature detection signal.

25   **BRIEF DESCRIPTION OF THE DRAWINGS**

The above and other objects, advantages and features of the present invention will be more apparent from the following detailed description taken with the attached drawings in which:

Fig. 1 is a schematic block view showing a period control 30 circuit for a self-refresh operation according to the present invention;

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Fig. 2 is a detailed circuit view showing a CBR mode detector shown in Fig. 1;

Fig. 3 is comprised of Figs. 3A and 3B, in which Fig. 3A is a detailed circuit view showing a voltage detector and Fig. 3B is a detailed circuit view showing a temperature detector shown in Fig. 1;

Fig. 4 is comprised of Figs. 4A to 4C, in which Fig. 4A is a detailed circuit view showing a pulse selector, Fig.4B is a detailed circuit view showing a self-refresh signal generator, and Fig. 4C is a detailed circuit view showing a master clock generator, shown in Fig.1 respectively;

Fig. 5 is a detailed circuit view showing a self-refresh enable signal generator shown in Fig. 1;

Fig. 6 is a detailed circuit view showing a reset signal generator shown in Fig. 1; and

Fig. 7 is an operational timing diagram of Fig. 1.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

In the following description, each detailed circuit, specific data, the number of the pulse trains, and each period of pulse train are used to bring a better understanding of the embodiment of the present invention. Moreover, it is well known to one skilled in the art to realize the present invention without specific and detailed disclosure of the elements.

A term "memory cell" used in the present invention means a dynamic memory cell comprised of one transistor and one capacitor, as well known.

Further, the well resistance represents a sheet resistance of an well region formed on a semiconductor substrate. Also, a polycrystalline silicon(in the following, called "polysilicon" for short) resistance represents the sheet resistance of the

polysilicon load formed on the semiconductor substrate.

Referring to Fig. 1, a self-refresh period control circuit according to present invention is comprised of the CBR mode ($\overline{CAS}$ Before $\overline{RAS}$ mode) detecting circuit 10 for outputting a timer driving signal ϕT_{mon} to enable the timer responding to the inverse low address strobe signal $\overline{RAS}$ and a inverse column address strobe signal $\overline{CAS}$; the pulse train generating circuit 12 for outputting a number of pulse trains QO-QN having different periods from each other responding to the timer driving signal ϕT_{mon}; a temperature and voltage detecting circuit 14 for outputting a temperature detection signal $\phi Tdet$ by detecting that the ambient temperature of the memory device reaches at a predetermined level and a voltage detection signal $\phi Vdet$ by detecting that the power supply voltage supplied to the memory device reaches at a predetermined level; a master clock generating circuit 16 for generating the new periodic combination pulse trains by combining the pulse trains output from the pulse train generating circuit 12 and for outputting any one of the new periodic combination pulse trains as a master clock signal ϕRd of the self-refresh operation; a self-refresh enable signal generator 18 for outputting a self-refresh enable signal ϕsre permitting a generation of the master clock signal ϕRd with a predetermined time delay after the timer driving signal ϕT_{mon} is activated; and a reset signal generator 20 for outputting a reset signal $\phi Reset$ under a predetermined condition.

Figs. 2 to 6 are detailed circuit views showing each of blocks included in Fig. 1.

Referring to Fig. 2, the CBR mode detecting circuit 10 is comprised of a ϕR generator 30 having five serially connected inverters which receive the inverse low address strobe signal $\overline{RAS}$ and output the signal ϕR; a ϕC generator 32 having five

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serially connected inverters which receive the inverse column address strobe signal $\overline{CAS}$ and output the signal ϕC; and a timer driving signal generator 34 which consists of two NAND gates 102 and 104 which receive the signals ϕR and ϕC as the respective

5   first inputs and receive mutual output signals as the respective second inputs, a NAND gate 106 which receives the signal ϕR as the first input and receives the output signal of the NAND gate 102 as the second input, and an inverter 108 for outputting the timer driving signal ϕT_{mon} by inverting the output signal of the NAND

10 gate 106. In Fig. 2, if the signal $\overline{RAS}$ goes to the logic low level (in the following, called "low level" for short) after the signal $\overline{CAS}$ went to the low level, the timer driving signal ϕT_{mon} is output as the logic high level (in the following, called "high level" for short) while the signals $\overline{CAS}$ and $\overline{RAS}$ are kept at

15 the low level.

The pulse train generating circuit 12 for outputting a number of frequency pulse trains Q0-QN having different periods from each other is comprised of a timer 36 and a frequency divider 38.

The timer 36 for outputting the pulse train ϕOSC being

20 controlled by the timer driving signal ϕT_{mon} output from the timer driving signal generator 34, uses a current mirror type ring-oscillator which can minimize the influence of an operating voltage and an ambient temperature. The detailed circuit view and the operational characteristics of the current mirror type ring-

25 oscillator is disclosed in pages 45 and 46 of the publication entitled "SYMPOSIUM ON VLSI CIRCUITS DIGEST OF TECHNICAL PAPERS" published in 1987.

Further, the frequency divider 38 which receives the pulse train signal ϕOSC output from the timer 36 and outputs a number

30 of the pulse trains Q0-QN having different periods from each other, uses a typical ripple counter, as well known to one skilled

in the art. Therefore, the period of pulse train Q0 is two times longer than the period of the ϕOSC, and also the period of pulse train Q1 is two times longer than the period of the pulse train Q0. Finally, the period of pulse train QN having the longest period is 2^{N+1} times longer than the period of the ϕOSC.

Referring to Fig. 3A, the voltage detector 40 consists of a voltage level detector 110, an output stage 112 and a detection controller 114. When the power voltage applied to the memory device has the higher level than a predetermined detecting voltage Vref, the voltage level detector 110 outputs the voltage detecting signal of the high level. Here, since the operation of voltage level detector 110 is well known in the art, the explanation will be omitted in the detailed description of the present invention. The output stage 112 consists of a CMOS transfer gate 120 transferring the output signal of the voltage level detector 110, a latch 122 for temporarily storing the output of the CMOS transfer gate 120, and an inverter 124 for outputting the voltage detection signal ϕVdet by inverting the output of the latch 122. The detection controller 114 consists of a NAND gate 118 which receives the timer driving signal ϕT_{mon} and a self-refresh signal srfhp (this will be explained in detail in Fig.4), and an inverter 116 for inverting the output signal of the NAND gate 118. The output signal of the inverter 116 and the inverse output signal of the output of the inverter 116 control an N channel gate and P channel gate of the CMOS transfer gate 120 respectively. Therefore, when the timer driving signal ϕT_{mon} and the self-refresh signal srfhp are kept at the high level, the CMOS transfer gate 120 is turned on, so that the output signal of the voltage level detector 110 is transferred to the output stage 112.

In Fig. 3, if the power supply voltage Vcc is higher than the detecting voltage Vref, the voltage level detector 110 outputs a signal having high level, so that the signal ϕVdet of the high

level is output to the output stage 112 when the output of the detection controller 114 is set to the high level. On the other hand, if the power supply voltage Vcc is lower than the detecting voltage Vref, the voltage level detector 110 outputs a signal of the low level, so that the signal ϕVdet of the low level is output to the output stage 112 when the output signal of the detection controller 114 is set to the high level. Therefore, whether the power supply voltage provided to the memory device is lower than a predetermined detecting voltage Vref or not, can be detected.

Next, referring to Fig. 3B, the temperature detector 42 consists of two NAND gates 126 and 128 for receiving the self-refresh signal srfhp as the respective first input signals via the four serially connected inverters UI1-UI4 and LI1-LI4, and for receiving the mutual output signal as the respective second input signals, a buffer stage 130 for receiving the output signal of the NAND gate 126, an output stage 112 for receiving the output signal of the buffer stage 130 and for outputting the temperature detection signal ϕTdet to the output node, and the detection controller 114 for controlling the detecting operation by selectively preventing the output signal of the buffer stage 130 from being transferred to the output stage 112. Since the output stage 112 and the detection controller 114 are the same as that of Fig. 3A, they are represented as the same number, so that the explanation will be omitted, here. The inverters UI1 and UI3 out of the four serially connected inverters UI1-UI4 which transfer the self-refresh signal srfhp to the first input signal of the NAND gate 126, are connected to a ground voltage terminal Vss via the resistors Rw1 and Rw3 respectively, and also the inverters UI2 and UI4 are connected to the power voltage terminal Vcc via the resistors Rw2 and Rw4 respectively. Further, the inverters LI1-LI3 out of the four serially connected inverters LI1-LI4 which transfer the self-refresh signal srfhp to the first input signal of the NAND gate 128, are connected to the ground voltage terminal

Vss via the resistors Rp1 and Rp3 respectively, and also, the inverters LI2 and LI4 are connected to the power voltage terminal Vcc via the resistors Rp2 and Rp4 respectively. The resistors Rw1-Rw4 are the well resistors and the resistors Rp1-Rp4 are the

5   polysilicon resistors.

In the following, the UI1-UI4 are called a first inverter group and the LI1-LI4 are called a second inverter group in order to easily explain the embodiment of the present invention.

Generally, as known in the art, the well resistor and poly
10 resistor have temperature-resistance coefficients different from each other. The inventor forms the well resistance and the polysilicon resistance on the same silicon substrate, and then the inventor obtained the result given in Table 1 by measuring the respective sheet resistance.

15   Table 1

Temperature	polysilicon resistor	well resistor
25°C	55.0 Ω/□	460.0 Ω/□
45°C	56.2 Ω/□	514.5 Ω/□
65°C	56.9 Ω/□	564.5 Ω/□
85°C	57.7 Ω/□	612.6 Ω/□
105°C	60.1 Ω/□	671.3 Ω/□

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As shown in Table 1, the variation ratio of resistance corresponding to the ambient temperature in well resistor is higher than that in the polysilicon resistor.

In Fig. 3B, the well resistors Rw1-Rw4 and the polysilicon resistors Rp1-Rp4 are formed that having a same resistance in the desired detecting temperature. The variation ratio of the well resistors Rw1-Rw4 corresponding to the ambient temperature are

5   higher than those of the polysilicon resistors Rp1-Rp4, so that the difference of the time delay between the first inverter group and the second inverter group is generated. If the ambient temperature is higher than the detecting temperature, the resistances of the well resistors Rw1-Rw4 are higher than those

10   of the polysilicon resistors Rp1-Rp4, thereby the time delay of the first inverter group is longer than that of the second inverter group. Therefore, when the self-refresh signal srfhp goes to the "high" level, the output signal of NAND gate 128 goes to "high" level earlier than the output signal of NAND gate 126, so

15   that the output signal of NAND gate 126 is latched to the "high" level, thus generating the temperature detection signal ϕTdet of the "high" level. On the contrary, if the ambient temperature is lower than the detecting temperature, the resistances of the well resistors Rw1-Rw4 are lower than those of the polysilicon

20   resistors Rp1-Rp4, thereby the time delay of the first inverter group is shorter than that of second inverter group. Therefore, when the self-refresh signal srfhp goes to the "high" level, the output signal of NAND gate 126 goes to "low" level earlier than the output signal of NAND gate 128, so that the output signal of

25   NAND gate 126 is latched to the "low" level, thus generating the temperature detection signal ϕTdet of the "low" level. Thus, whether the ambient temperature of the memory device is higher than a predetermined detecting temperature or not, can be detected.

30   Referring to Fig. 4A, the pulse selector 44 consists of NAND gates 132-146, 160 and NOR gates 148-158. A NAND gate 132 receives the inverted voltage detection signal ϕ $\overline{\text{Vdet}}$ and the inverted temperature detection signal ϕ $\overline{\text{Tdet}}$, a NAND gate 134 receives the

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voltage detection signal ϕVdet and the inverted temperature detection signal ϕ $\overline{\text{Tdet}}$, a NAND gate 136 receives the inverted voltage detection signal ϕ $\overline{\text{Vdet}}$ and the temperature detection signal ϕTdet, and a NAND gate 138 receives the voltage detection

5 signal ϕVdet and the temperature detection signal ϕTdet. A NAND gate 140 receives the pulse trains Q3 and Q5, a NAND gate 142 receives the pulse trains Q3 and Q6, a NAND gate 144 receives the pulse trains Q2 and Q5, and a NAND gate 146 receives the pulse trains Q0 and Q6. A NOR gate 148 receives the output signals of

10 the NAND gates 132 and 140, a NOR gate 150 receives the output signals of the NAND gates 134 and 142, a NOR gate 152 receives the output signals of the NAND gates 136 and 144, and a NOR gate 154 receives the output signals of the NAND gates 138 and 146. A NOR gate 156 receives the output signals of the NOR gates 148 and 150,

15 a NOR gate 158 receives the output signals of the NOR gates 152 and 154. A NAND gate 160 receives the output signals of the NOR gates 156 and 158, to output a signal ϕsrp.

Referring to Fig. 4B, the self-refresh signal generator 46 consists of a NOR gate 164 receiving the signal ϕsrp as a first

20 input and the signal ϕsrp, as a second input, inverted and time-delayed by the seven serially connected inverters 162, and a inverter 166 receiving the output signal of NAND gate 164 and outputting the self-refresh signal srfhp. It is preferable that the time delay by the inverter 162 should coincide with the random

25 read or write cycle time t_{RC} of the memory device. Thus, if the signal ϕsrp goes to the "low" level from the "high" level, the output signal of the NOR gate 164 goes to the "high" level during the random read or write cycle time t_{RC}.

Referring to Fig. 4C, the master clock generator 48 consists

30 of an inverter 168 for receiving a self-refresh enable signal ϕsre, a NAND gate 170 for receiving the output signal of the inverter 168 and the signal ϕR, a NOR gate 172 for receiving the

output signal of the inverter 168 and the signal srfhp, an inverter 174 for inverting the output signal of the NOR gate 172, a NAND gate 176 for receiving the output signal of the NAND gate 170 and the output signal of the inverter 174, and an output

5 buffer 178 for outputting the master clock signal ϕRd by receiving the output signal of the NAND gate 176. In Fig. 4C, when the signal ϕR and the signal ϕsre are kept at the "high" level, the master clock signal ϕRd becomes the inverted signal of the self-refresh signal srfhp. Therefore, the generation of the master

10 clock signal ϕRd is controlled by the self-refresh enable signal ϕsre.

Fig. 5 is a detailed circuit view showing the self-refresh enable signal generator 18 shown in Fig. 1. After advancing to the CBR mode, the self-refresh enable signal should be enabled after

15 a lapse of a predetermined time. In Fig. 5, though the timer driving signal ϕT_{mon} changes to the "high" level, if the pulse Qi is not enabled to the "high" level, the self-refresh enable signal ϕsre is kept at the "low" level. Meanwhile, in this state, if the pulse Qi is enabled to the "high" level, the signal ϕsre is kept

20 at the "high" level while the signal ϕT_{mon} is kept at the "high" level.

Fig. 6 is a detailed circuit view showing the reset signal generator 20 shown in Fig. 1. The reset signal generator 20 consists of a NAND gate 200 for receiving the self-refresh enable

25 signal ϕsre as a first input and the self-refresh signal srfhp, as a second input, via an inverter 198, a NAND gate 204 for receiving the output signal of the NAND gate 200 as a first input and the output signal of the NAND gate 200, as a second input, time-delayed and inverted by five serially connected inverters

30 202, a NAND gate 206 for receiving the output signal of the NAND gate 204 and the timer driving signal ϕT_{mon}, and an inverter 208 for outputting the reset signal ϕReset by inverting the output

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signal of the NAND gate 206. The timer driving signal ϕT_{mon} inputting to the NAND gate 206 controls the generation of the reset signal. When the timer driving signal $\phi Tmon$ and the signal ϕsre are kept at the "high" level, if the self-refresh signal

5   srfhp goes to the "low" level, the output signal of the NAND gate 200 becomes the "low" level for the delay time by the inverters 202. The reset signal resets the frequency divider 38.

Fig. 7 shows a timing diagram of the circuit according to the present invention. References will now be made to Figs. 4 to 7 to

10   bring a better understanding of the period selecting operation of the circuit in Fig. 1.

In the following descriptions, it is assumed for the sake of explanation that a period of the pulse train ϕOSC supplied from the timer 36 is $2\mu sec$ and the pulse train ϕOSC is sequentially

15   frequency-divided by the frequency divider 38, thus generating frequency-divided pulse trains Q0-Q7 of which periods are as described in Table 2. It is further assumed that the total number of the rows (i.e., the number of the word lines to be driven) to be refreshed for one refresh cycle is 2,048 and the data retention

20   time of the memory cells according to the voltage level and the temperature level is as described in Table 3. In Table 3, when the voltage supplied to the memory device is lower than a predetermined reference level and the ambient temperature of the memory device is higher than a predetermined reference temperature

25   (i.e., the memory device operates under the worst operating condition), the data retention time of the memory cells is 170msec, so that 2,048 rows must be completely refreshed within the data retention time of 170msec. Alternatively, when the voltage supplied to the memory device is higher than the

30   predetermined reference level and the ambient temperature of the memory device is lower than the predetermined reference voltage (i.e., the memory device operates under the best operating

condition), the data retention time of the memory cells is 340msec, so that the memory device must refresh 2,048 rows completely within the data retention time of 340msec.

Table 2

Pulse Train	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Period	4μs	8μs	16μs	32μs	64μs	128μs	256μs	512μs

Table 3

	Case 1	Case 2	Case 3	Case 4
Detection Signal Levels	ϕVdet:L ϕTdet:H	ϕVdet:L ϕTdet:L	ϕVdet:H ϕTdet:H	ϕVdet:H ϕTdet:L
Data Retention Time (ms)	170	210	280	340
Combination of Pulse Trains	Q2 + Q5	Q3 + Q5	Q0 + Q6	Q3 + Q6
Period of Master Clock ϕRd	80	96	132	160
Refresh Cycle Time (ms)	163.8	196.6	270.3	160

Descriptions will now be given on the operations of the self-refresh period control circuit of Fig. 1 under the condition of the case 4 in Table 3, in which the voltage detection signal ϕVdet from the voltage detector 40 is the "high" level and the temperature detection signal ϕTdet from the temperature detector 42 is the "low" level, respectively.

Referring back to Fig. 1, as going into the CBR mode, the timer driving signal ϕTmon changes to the "high" level and, accordingly, the timer 36 generates the pulse train ϕOSC. The frequency-divider 38 frequency-divides the pulse train ϕOSC to

generate the pulse trains Q0-Q7, which are then applied to the pulse selector 44. Referring to Fig. 5, after a lapse of a predetermined time, for example 200μsec, determined by the clock Qi, the memory device advances to the self-refresh mode at a time t0 when the self-refresh enable signal ϕsre from the self-refresh enable signal generator 18 goes to the "high" level. At this moment, as shown in Fig. 2, the signal ϕR maintains the "high" level according to the $\overline{RAS}$ signal activated to the "low" level. As a result, in the self-refresh mode, the signal ϕR, the self-refresh enable signal ϕsre and the timer driving signal ϕTmon are all maintained at the "high" level.

With reference to Fig. 4A, since the voltage detection signal ϕVdet is at the "high" level and the temperature detection signal ϕTdet is at the "low" level, only the output of the NAND gate 134 goes to the "low" level and the outputs from the remaining NAND gates 132, 136 and 138 are all at the "high" level. Accordingly, since only a combination pulse train Q3+Q6 output from the NAND gate 142 receiving the pulse trains Q3 and Q6 is valid and the other remaining combination pulse trains are all neglected, the signal ϕsrp output from the NAND gate 160 become the combination pulse train Q3+Q6. Therefore, the signal ϕsrp has the "high" level at a time between t1 and t2 at which the pulse trains Q3 and Q6 are simultaneously the "high" level.

The signal ϕsrp is changed to the self-refresh signal srfhp at the self-refresh signal generator 46 shown in Fig. 4B. In Fig. 4B, since the number of the serially connected inverters 162 is odd number (seven in Fig. 4B), the self-refresh signal srfhp maintaining the "low" level between the time t2 and the time t3 delayed by the inverters 162 is generated at the time t2 at which the signal ϕsrp changes from the "high" level to the "low" level.

Referring to Fig. 4C, since the signal ϕR and the self-

refresh enable signal ϕsre are all maintained at the "high" level, the master clock generator 48 inverts the self-refresh signal srfhp to generate the master clock ϕRd.

It is well known in the art that the master clock ϕRd
controls the RAS chain of the memory device, and internal
addresses generated under the control of the master clock drives
a selected one of 2,048 word lines. Such an operation is repeated
for the every generation of the master clock to refresh the entire
memory cells.

Referring to Fig. 6, since the self-refresh enable signal
ϕsre and the timer driving signal ϕTmon maintain the "high" level,
the reset signal ϕReset having the "low" level for the delay time
by the serially connected inverters 202 is generated at a time t3
at which the self-refresh signal srfhp changes from the "low"
level to the "high" level. Therefore, the frequency divider 38
shown in Fig. 1 is reset and, accordingly, the pulse trains Q0-Q7
output from the frequency divider 38 are all initialized to
generate the pulse trains having the same states as those at the
time t0.

The above described operations are repeated as long as the
voltage detection signal ϕVdet and the temperature detection
signal ϕTdet are at the "high" level and the "low" level,
respectively. That is, the pulse trains Q0-Q7, the signal ϕsrp,
the self-refresh signal srfhp and the master clock ϕRd are
sequentially generated from the time t0 to the time t3 and thus,
the second active pulse of the master clock ϕRd is generated at
a time t4, repeatedly performing the same operation.

The time interval between the time t2 and the time t3 for
which the master clock ϕRd is activated to the "high" level
approximates to the random read/write cycle time t_{RC} of the memory

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device. Thus, this time interval is negligible when compared with the total refresh operation time. Accordingly, a period of the master clock ϕRd defined as the time interval between the time t3 and the time t4 approximates to a period (160μsec) of the combination pulse trains Q3+Q6. The time for which a selected one of the word lines is refreshed after a previous word line is refreshed, i.e., the refresh cycle time is 160x2,048$\approx$327.7msec. Thus, the refresh cycle time 327.7msec satisfies the data retention time 340msec of the memory cells.

In the voltage detector 40 of Fig. 3A, the "high" level is generated from the detection controller 114 every time when the self-refresh signal srfhp changes from the "low" level to the "high" level, so as to turn on the transfer gate 120 of the output stage 112. The output stage 112 generates a new voltage detection signal ϕVdet at the time when the self-refresh signal changes from the "low" level to the "high" level (i.e., when the master clock changes from the "high" level to the "low" level). In similar, the temperature detector 42 of Fig. 3B generates a new temperature detection signal at a time when the self-refresh signal srfhp changes from the "low" level to the "high" level.

Accordingly, the voltage detector 40 of Fig. 3A and the temperature detector 42 of Fig. 3B respectively detect the supply voltage and the ambient temperature at a time when the master clock ϕRd is inactivated to the "low" level after an activation of the "high" level. Thus, in the pulse train selector 44 of Fig. 4A, a selected one of the NAND gates 132, 134, 136 and 138 generates an output signal of the "low" level according to the new voltage detection signal ϕVdet and the new temperature detection signal ϕTdet, so that one of the four combination pulse trains is selected to generate the signal ϕsrp.

For example, in the course of the operation under the

condition of the case 4, if the supply voltage is maintained constantly while the ambient temperature increases more and more, the voltage detection signal ϕVdet and the temperature detection signal ϕTdet are all at the "high" level, thereby advancing to a

5   condition of the case 3 of Table 3. Under the condition of the case 3, in the pulse selector 44 of Fig 4A, the NAND gate 138 generates the "low" level and the remaining NAND gates 132, 134 and 136 generate the "high" level, in response to the detection signals, thereby selecting the combination pulse train Q0+Q6 to

10   generate the signal ϕsrp. Therefore, the period of the master clock ϕRd becomes 132μsec which is the period of the combination pulse train Q0+Q6. Thus, the refresh cycle time is 132x2,048≒270.3msec, thereby satisfying the data retention time of 280msec under the case 3.

15   Operations under the conditions of the case 1 and case 2 also will be readily appreciated from the above descriptions concerning the case 4 and case 3.

As shown in Table 3, the self-refresh period control circuit according to the present invention can generate the combination

20   pulse trains having variable periods, so that a master clock having a period approximating to the data retention time is generated. Therefore, the unnecessary self-refresh operations are prevented during the standby state, thus reducing the current consumptions.

25   Further, the self-refresh period control circuit according to the present invention automatically controls the self-refresh period according to the variations of the power supply voltage and the ambient temperature, so that the self-refresh operation may be optimized.

30   In the above mentioned embodiment, the period of the self-

refresh operation was obtained by using the pulse selecting part
shown in Fig. 4A. According to the another embodiment of the
present invention, any one of the pulse trains provided from the
divider can be selected, in response to the voltage detect signal
5 and the temperature detect signal.

Further, the period of the self-refresh operation can be
controlled by making the number of the voltage detecting part and
the temperature detecting part various, in response to the closer
changes of the temperature and the voltage.